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# 2N4918 thru 2N4920*

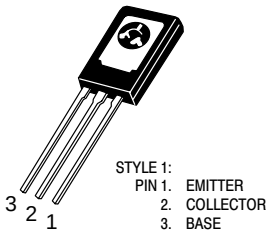
*ON Semiconductor Preferred Device

# Medium-Power Plastic PNP Silicon Transistors

. . . designed for driver circuits, switching, and amplifier applications. These high–performance plastic devices feature:

- Low Saturation Voltage — $V_{CE(sat)}$ = 0.6 Vdc (Max) @ $I_C$ = 1.0 Amp
- Excellent Power Dissipation Due to Thermopad Construction — $P_D$ = 30 W @ $T_C$ = 25°C
- Excellent Safe Operating Area
- Gain Specified to $I_C$ = 1.0 Amp
- Complement to NPN 2N4921, 2N4922, 2N4923

**3 AMPERE GENERAL–PURPOSE POWER TRANSISTORS 40–80 VOLTS 30 WATTS**




**CASE 77–09 TO–225AA TYPE**

***MAXIMUM RATINGS**

| Ratings | Symbol | 2N4918 | 2N4919 | 2N4920 | Unit |
|---|---|---|---|---|---|
| Collector–Emitter Voltage | $V_{CEO}$ | 40 | 60 | 80 | Vdc |
| Collector–Base Voltage | $V_{CB}$ | 40 | 60 | 80 | Vdc |
| Emitter–Base Voltage | $V_{EB}$ | 5.0 | | | Vdc |
| Collector Current — Continuous (1) | $I_C$* | 1.0<br>3.0 | | | Adc |
| Base Current | $I_B$ | 1.0 | | | Adc |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 30<br>0.24 | | | Watts<br>W/°C |
| Operating & Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –65 to +150 | | | °C |

**THERMAL CHARACTERISTICS (2)**

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Case | $\theta_{JC}$ | 4.16 | °C/W |

*Indicates JEDEC Registered Data for 2N4918 Series.

(1) The 1.0 Amp maximum $I_C$ value is based upon JEDEC current gain requirements. The 3.0 Amp maximum value is based upon actual current–handling capability of the device (See Figure 5).

(2) Recommend use of thermal compound for lowest thermal resistance.

**Preferred** devices are ON Semiconductor recommended choices for future use and best overall value.

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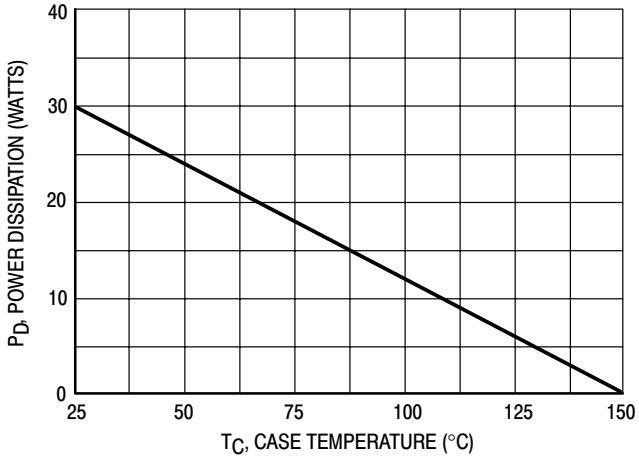



**Figure 1. Power Derating**

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector–Emitter Sustaining Voltage (1)<br>($I_C$ = 0.1 Adc, $I_B$ = 0) | 2N4918<br>2N4919<br>2N4920 | $V_{CEO(sus)}$ | <br>40<br>60<br>80 | <br>—<br>—<br>— | Vdc |
| Collector Cutoff Current<br>($V_{CE}$ = 20 Vdc, $I_B$ = 0)<br>($V_{CE}$ = 30 Vdc, $I_B$ = 0)<br>($V_{CE}$ = 40 Vdc, $I_B$ = 0) | <br>2N4918<br>2N4919<br>2N4920 | $I_{CEO}$ | <br>—<br>—<br>— | <br>0.5<br>0.5<br>0.5 | mAdc |
| Collector Cutoff Current<br>($V_{CE}$ = Rated $V_{CEO}$, $V_{BE(off)}$ = 1.5 Vdc)<br>($V_{CE}$ = Rated $V_{CEO}$, $V_{BE(off)}$ = 1.5 Vdc, $T_C$ = 125°C | | $I_{CEX}$ | <br>—<br>— | <br>0.1<br>0.5 | mAdc |
| Collector Cutoff Current<br>($V_{CB}$ = Rated $V_{CB}$, $I_E$ = 0) | | $I_{CBO}$ | — | 0.1 | mAdc |
| Emitter Cutoff Current<br>($V_{BE}$ = 5.0 Vdc, $I_C$ = 0) | | $I_{EBO}$ | — | 1.0 | mAdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (1)<br>($I_C$ = 50 mAdc, $V_{CE}$ = 1.0 Vdc)<br>($I_C$ = 500 mAdc, $V_{CE}$ = 1.0 Vdc)<br>($I_C$ = 1.0 Adc, $V_{CE}$ = 1.0 Vdc) | | $h_{FE}$ | <br>40<br>30<br>10 | <br>—<br>150<br>— | — |
| Collector–Emitter Saturation Voltage (1)<br>($I_C$ = 1.0 Adc, $I_B$ = 0.1 Adc) | | $V_{CE(sat)}$ | — | 0.6 | Vdc |
| Base–Emitter Saturation Voltage (1)<br>($I_C$ = 1.0 Adc, $I_B$ = 0.1 Adc) | | $V_{BE(sat)}$ | — | 1.3 | Vdc |
| Base–Emitter On Voltage (1)<br>($I_C$ = 1.0 Adc, $V_{CE}$ = 1.0 Vdc) | | $V_{BE(on)}$ | — | 1.3 | Vdc |
| **SMALL–SIGNAL CHARACTERISTICS** | | | | | |
| Current–Gain — Bandwidth Product ($I_C$ = 250 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 MHz) | | $f_T$ | 3.0 | — | MHz |
| Output Capacitance ($V_{CB}$ = 10 Vdc, $I_E$ = 0, f = 100 kHz) | | $C_{ob}$ | — | 100 | pF |
| Small–Signal Current Gain ($I_C$ = 250 mAdc, $V_{CE}$ = 10 Vdc, f = 1.0 kHz) | | $h_{fe}$ | 25 | — | — |

*Indicates JEDEC Registered Data.
(1) Pulse Test: PW ≈ 300 μs, Duty Cycle ≈ 2.0%

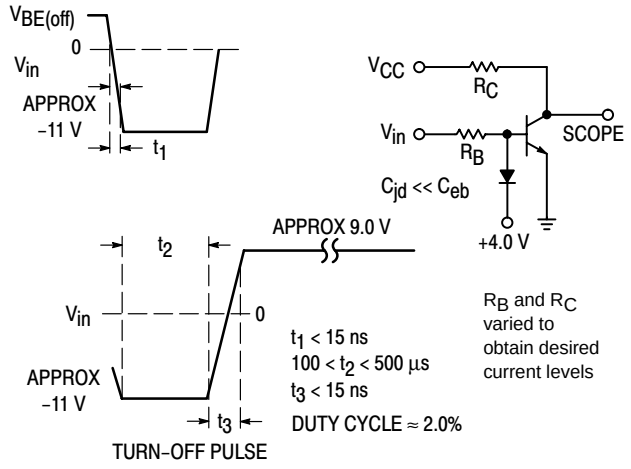



**Figure 2. Switching Time Equivalent Test Circuit**

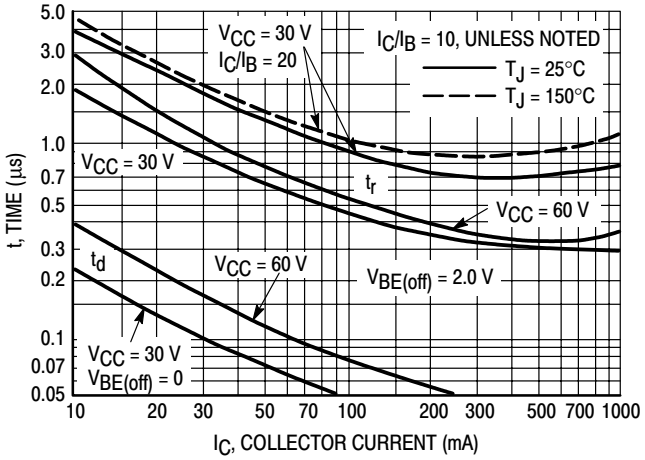



**Figure 3. Turn–On Time**

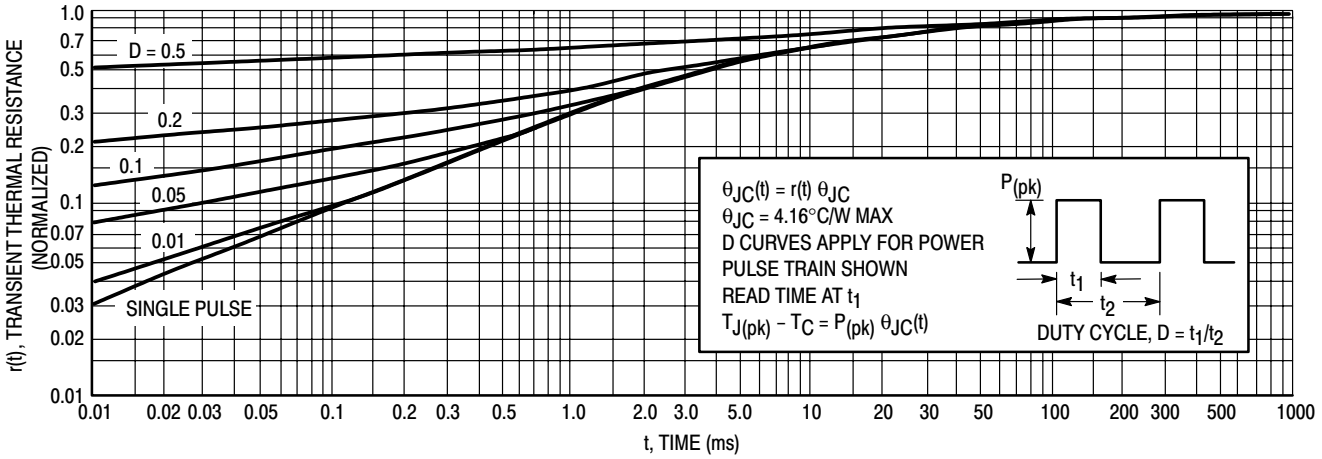



**Figure 4. Thermal Response**

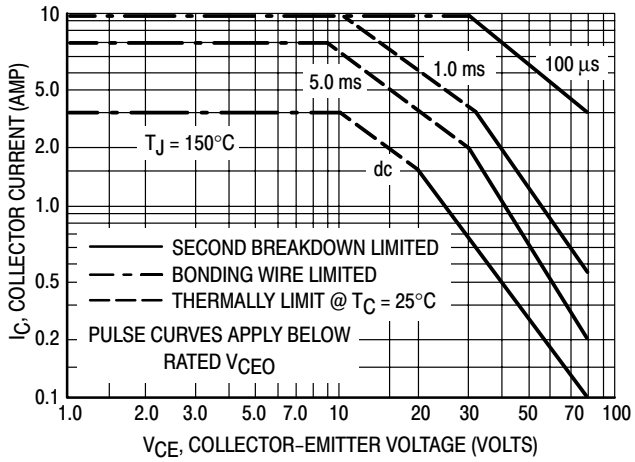



**Figure 5. Active−Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; $T_C$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150°C$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

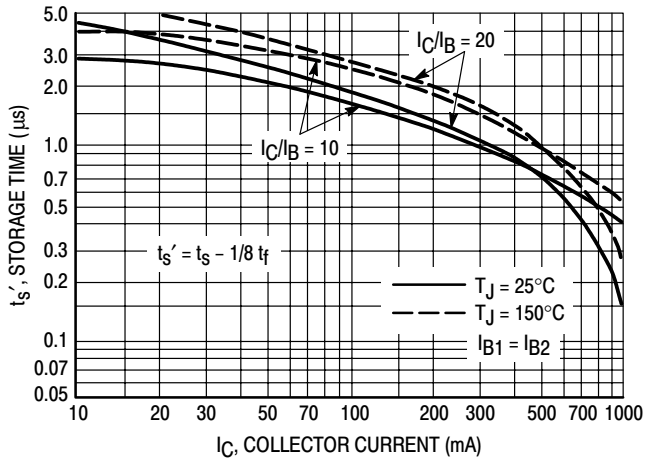



**Figure 6. Storage Time**

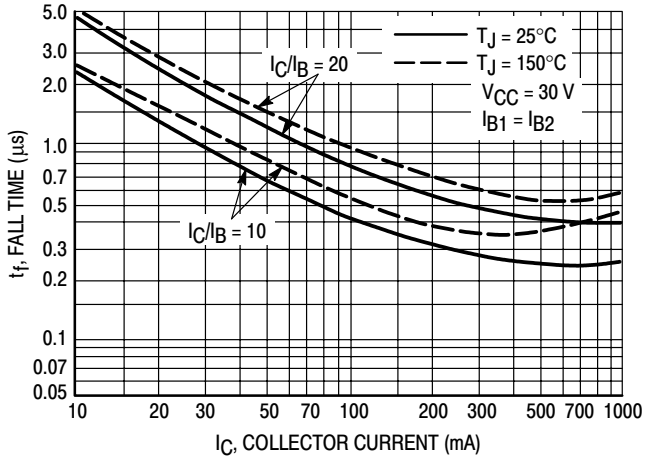



**Figure 7. Fall Time**

## TYPICAL DC CHARACTERISTICS

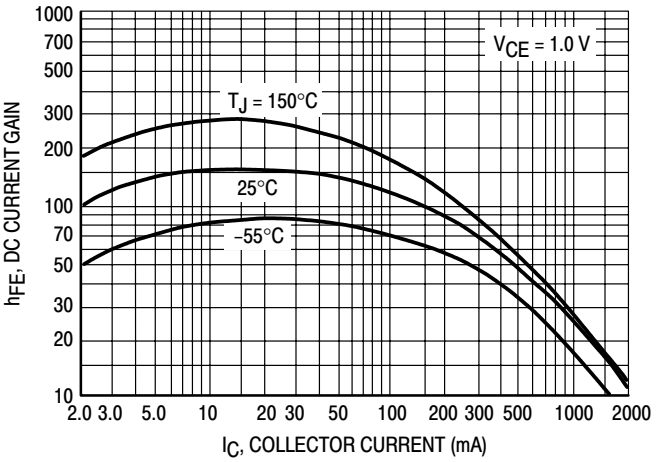



**Figure 8. Current Gain**

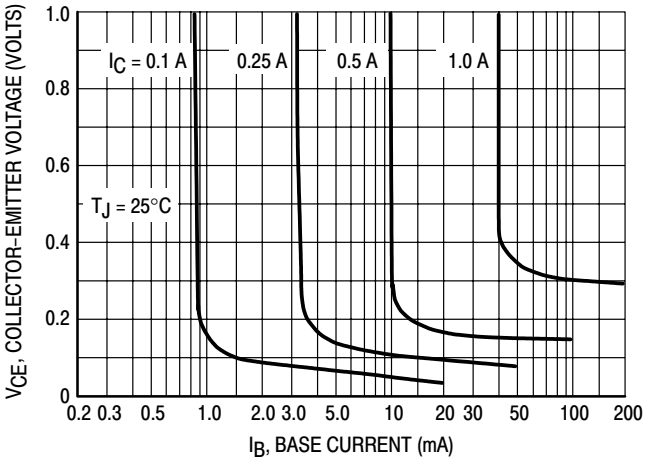



**Figure 9. Collector Saturation Region**

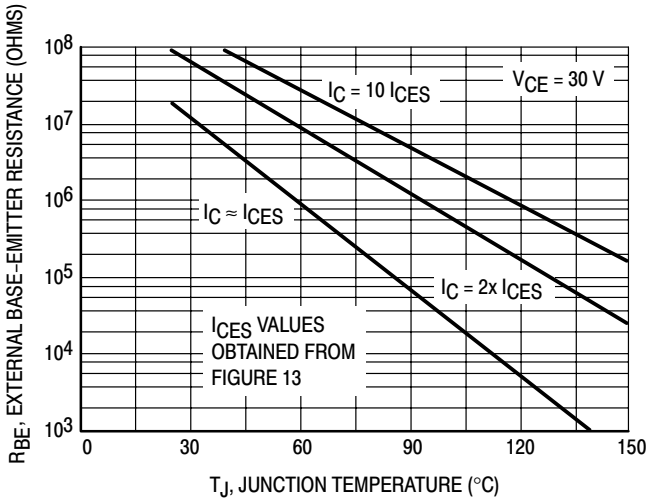



**Figure 10. Effects of Base−Emitter Resistance**

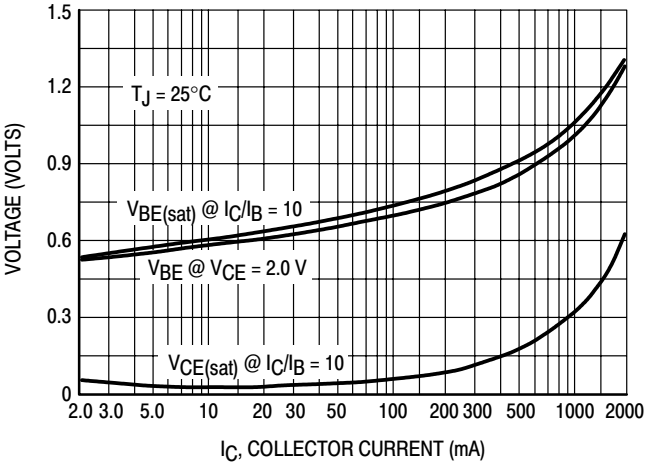



**Figure 11. "On" Voltage**

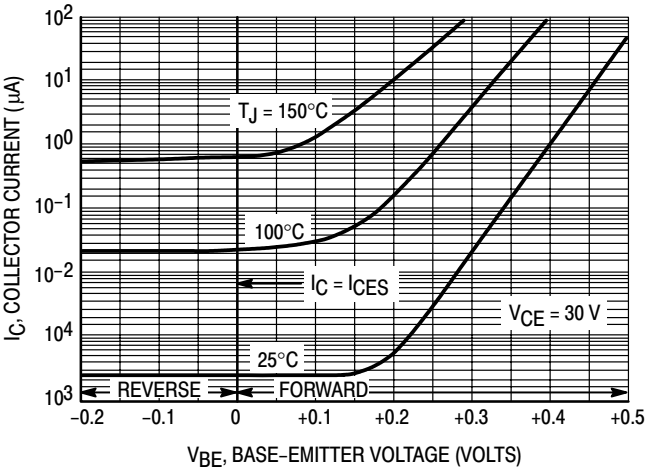



**Figure 12. Collector Cut−Off Region**

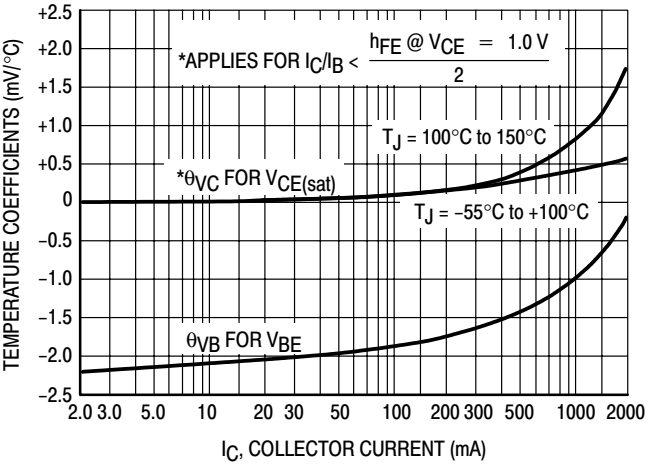
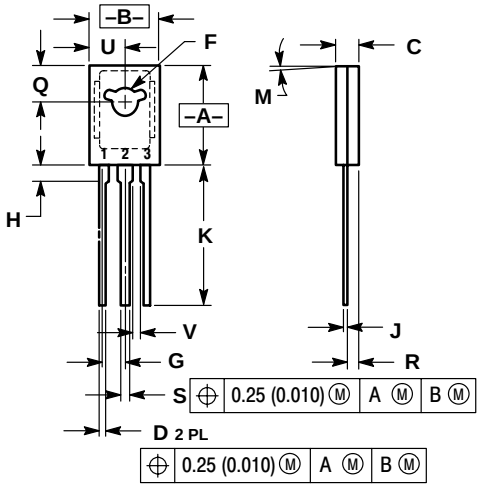

*APPLIES FOR $I_C/I_B$ < $\frac{h_{FE} @ V_{CE} = 1.0 V}{2}$
$T_J$ = 100°C to 150°C
*$\theta_{VC}$ FOR $V_{CE(sat)}$
$T_J$ = −55°C to +100°C
$\theta_{VB}$ FOR $V_{BE}$
TEMPERATURE COEFFICIENTS (mV/°C)
$I_C$, COLLECTOR CURRENT (mA)

**Figure 13. Temperature Coefficients**

## PACKAGE DIMENSIONS

**TO−225AA**
**CASE 77−09**
**ISSUE W**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.425 | 0.435 | 10.80 | 11.04 |
| B | 0.295 | 0.305 | 7.50 | 7.74 |
| C | 0.095 | 0.105 | 2.42 | 2.66 |
| D | 0.020 | 0.026 | 0.51 | 0.66 |
| F | 0.115 | 0.130 | 2.93 | 3.30 |
| G | 0.094 BSC | | 2.39 BSC | |
| H | 0.050 | 0.095 | 1.27 | 2.41 |
| J | 0.015 | 0.025 | 0.39 | 0.63 |
| K | 0.575 | 0.655 | 14.61 | 16.63 |
| M | 5° TYP | | 5° TYP | |
| Q | 0.148 | 0.158 | 3.76 | 4.01 |
| R | 0.045 | 0.065 | 1.15 | 1.65 |
| S | 0.025 | 0.035 | 0.64 | 0.88 |
| U | 0.145 | 0.155 | 3.69 | 3.93 |
| V | 0.040 | --- | 1.02 | --- |

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

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